



# V Rose Microsystems, Inc.

www.vrosemicrosystems.com

**VRM-AMC-V5Fe**

## Product Data Sheet

### Overview:

The VRM-AMC-V5Fe is a single width Advanced Mezzanine Card, mid or full-size depending on configuration. It is aimed at the latest applications requiring high performance FPGA processing and I/O, and also offers advanced capabilities in wireless and clock synchronisation should the application require this.

A Xilinx Virtex-5 LX110T FPGA provides the main processing. This configures and boots from FLASH on reset, using one of 4 selectable configuration images which are customer programmable and can be updated over Ethernet. The FPGA is fully customer configurable. The FPGA build may contain a MicroBlaze processor for basic board configuration and control, and a full example FPGA build and MicroBlaze Board Support Package is provided.

A 4x PCI Express interface is a key feature of the AMC-V5Fe, allowing low latency connection to a wide range of MicroTCA systems and CPUs. In addition there is a range of I/O provided including optical and serial interfaces with flexible clock synchronisation. A mezzanine site allows selected customers to add custom I/O or processing to the board if required. A range of build options are available, and further customisation is possible in volume, to enable the best technical and commercial fit to a customer application to be achieved.



### Features:

**FPGA:** Xilinx Virtex-5 FPGA. Standard configuration is LX110T-2, options include SX95T, LX155T. With:

- 2 independent banks of 128Mbytes x 16 DDR2-600 SDRAM
- 128Mbytes of parallel FLASH
- 8Gbps 1x or 4x PCI Express connected to AMC ports(4-7)
- 2 Full-duplex Gigabit Ethernet ports
- 4x RocketIO to front panel 10Gbps CX4 connector, option to AMC ports 17-20

**Optical Interface:** 2 SFP sockets for optical CPRI RE/REC and OBSAI RP3-01 compliant antenna interface links, connected to FPGA RocketIO. Also usable for optical links such as sFPDP, FC, SRIO, GigE. Data rate up to 3.75Gbps per link.

**Clock Synchronization:** Low-jitter OCXO based PLL, digitally controlled from the FPGA. Allows clock synchronization and distribution from an external 30.72 MHz or 1PPS GPS clock via AMC backplane, front panel (option) or SFP SERDES. IEEE1588 is also possible.

**Serial RapidIO:** 10Gbps 4x infrastructure using Tundra Tsi578 switch:

- AMC.4 Compliant 10Gbps 4x connections to AMC ports 4-7 and 8-11
- Dedicated 10Gbps 4x link to FPGA
- Optional Front Panel 10Gbps 4x SRIO link using CX4 connector

**Ethernet:** Gigabit Ethernet infrastructure using Broadcom BCM5389 switch:

- AMC.2 (1000BASE-BX) compliant connections to AMC Ports 0 & 1
- Full-duplex 1Gbps links

**IPMI:** ATmega128 IPMI controller:

- AMC.0 IPMB\_L interface
- FRU EEPROM data
- Power and reset control
- Real-Time health monitoring

**Form Factor:** Advanced Mezzanine Card

- AMC.0 Rev 2.0 compliant
- Mid-size, single-width; also available as full-size on request
- For AdvancedTCA and MicroTCA
- AMC.2 GigE and AMC.4 4x SRIO
- Hot swap support

**Environmental/Safety:**

- Operating Temp: 0—40C
- Power consumption: 28W Max
- 2004/108/EC and FCC EMC compliant
- 2002/95/EC RoHS, 2002/96/EC WEEE and 2006/95/EC Low voltage Directive Compliant



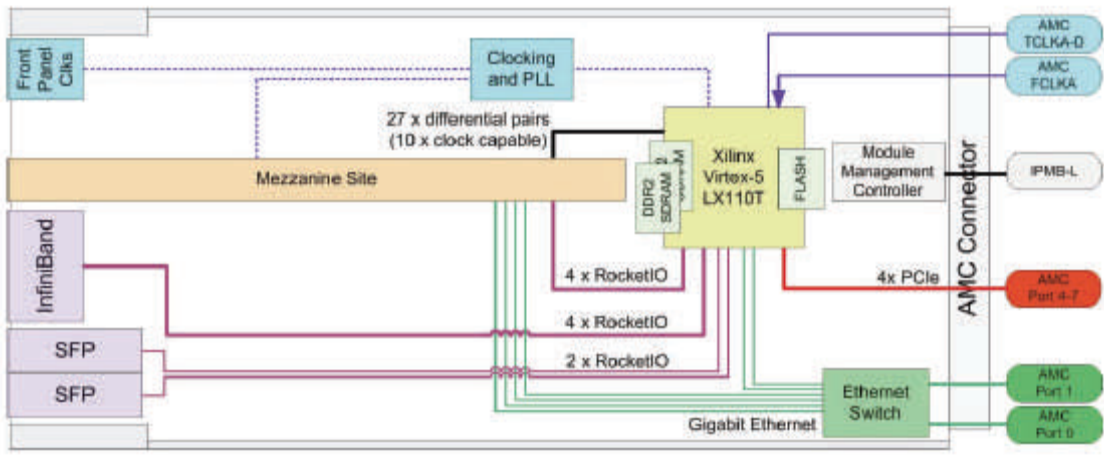
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### Block Diagram:



### Ordering:

**VRM-AMC-V5Fe:** Single width mid-size Advanced Mezzanine Card